Q&A with The MathWorks

Daily Briefing: *News Snippets*

Military EMBEDDED SYSTEMS

VOLUME 6 NUMBER 1
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INCLUDING:

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Core i7 storms the beaches

Also:

EOL: It's the end … or is it?

Top technologies for the warfighter

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Military EMBEDDED SYSTEMS

January/February 2010 Volume 6 Number 1

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Technology: Get it *into* your system

Mil Tech Trends: It's the end ... or is it?

ON THE COVER:

Storming the beaches: The U.S. Army's First Division goes ashore at Omaha Beach on 6 June 1944 for the D-Day invasion. At great loss of life under withering fire from the ground, artillery, and air, Allied Forces establish a beachhead along the French coast. It would take another year before World War II was officially declared won (see story, page 15).

In the new decade that started 1 January 2010, Intel is establishing itself as the dominant force in military microprocessors. From 2008's Atom processor to the new Nehalem ISA in the Intel Core Technology family (Core i7, i5, and i3), rare will be the defense system that doesn't use an Intel CPU. Surprisingly, the Core family also has stunning DSP performance and stands poised to drive back the PowerPC's AltiVec in signal processing and other DSP applications. See stories on pages 20 and 42.

Image courtesy of the U.S. Coast Guard as taken by Chief Photographer's Mate (CPHOM) Robert F. Sargent, U.S. Coast Guard, 1944.

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VITA 65 clarifies VPX interoperability profiles

By Duncan Young

New defense and aerospace embedded computing implementations are rapidly migrating from VMEbus to VPX (VITA 46), and the rate of adoption is rising. VPX offers the systems integrator new levels of architectural and performance potential with an abundance of multi-GHz signaling connectivity in proven 3U and 6U packaging standards. However, VPX's inherent flexibility highlights the need for vendors of modules and backplanes to classify product capabilities in a common way and move closer to universal interoperability. OpenVPX (VITA 65) clarifies the way that products should be classified, thus ensuring, for example, that modules meeting a declared profile are compatible with a backplane slot supporting that profile, and so on.

Architectural convention

But VITA 65 is not intended to succeed or replace VPX. Its purpose is to guide the systems integrator toward a viable, interoperable, single- or multi-vendor VPX-based solution. Of necessity, VITA 65 creates an architectural convention representing a consensus of current practice. This convention cannot be fixed forever and might be superseded by new technology as it is introduced into VPX products. As a result, VITA 65 can continuously evolve at the rate of innovation and technology introduction, and planes – along with pipes and modules – are essential ingredients.

Planes

An interoperable system is two or more modules plugged into a backplane providing the interconnect between the modules, plus power supplies and a means of thermal management. Architecturally, a VITA 65 system's interconnections and intramodule communications are characterized by planes and pipes. Five planes are defined: a control plane, traditionally the role for VMEbus but now supplanted by Ethernet; a data plane for intramodule data transfer; an expansion plane for I/O, other types of data movement, or data storage; a management plane (chassis level); and a utility plane (slot level). The control, data, and expansion planes might currently be combinations of Serial RapidIO, PCI Express, or Ethernet, with much of the detail and options available for all five planes already defined by VITA 46 and its dot specifications.

Pipes and modules

Pipes are groups of differential pairs classified only by the number of pairs per pipe. They would typically be used in an application for Serial RapidIO or PCI Express. The definition of pinout is from the relevant VITA 46 dot specifications. Pipes are classified in VITA 65 by their size, from an Ultra Thin Pipe (UTP) with two differential pairs to an Octal Fat Pipe (OFP) with 64 pairs, plus rules for how a module or backplane will support one, two, or none of them. And, finally, VITA 65 defines four slot and module profiles that include a switch, a bridge, a payload (for example, an SBC), or a peripheral. VITA 65 profiles will be created for slots, backplanes, and module types; the pipes and the protocols they support; plus slot size and cooling methodology. To implement a practical application with specific functional and performance requirements, developers can select modules to meet these requirements: Their VITA 65 profiles will lead to slot profiles which, in addition to the system's architectural needs, will lead to a compatible backplane profile.

It is anticipated that as the market develops, certain profiles will predominate, certainly for laboratory development systems. However, the nature of the VPX market, which is mainly military and industrial, is such that implementations are very closely matched to specific applications, often to optimize Size, Weight, and Power (SWaP). These markets use much special-to-type I/O; hence, VITA 65 makes no recommendations for use of the *user-defined* pins. As a participant in the development of the VITA 65 standard, GE Intelligent Platforms offers a number of 3U and 6U VPX payload and switch products that meet its classification criteria. One of these is the DSP230 quad depicted in Figure 1.

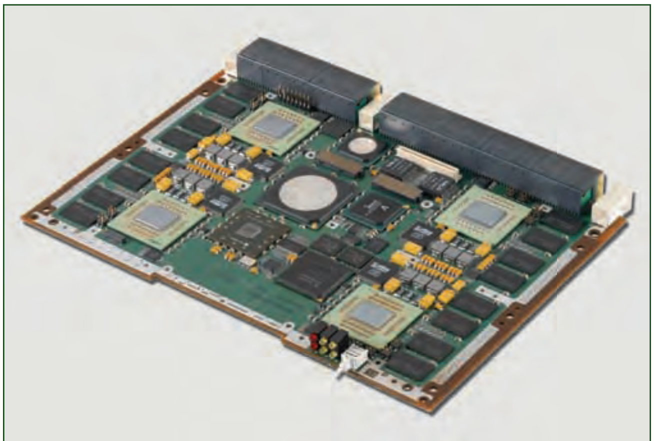

Figure 1 | DSP230 multiprocessor blade from GE Intelligent Platforms

VITA 65 is intended to be a living, breathing document, expanding with market and technology growth, but also able to accommodate deletions or modifications of existing profiles as their usage or applicability changes. VITA 65 brings clarity to the system builder by assuring interoperability of products offered by a broad vendor base while offering those vendors broad enough scope to sustain product differentiation, encourage innovation, and prevent the stagnation of future technology development.

To learn more, e-mail Duncan at young.duncan1@btinternet.com.

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Contractors look for higher levels of integration from COTS suppliers

By Steve Edwards

As COTS embedded computing products continue to evolve, they become more complex with levels of performance and functionality that often require specialized skills and knowledge to integrate most effectively as part of a prime contractor's deliverable system. A typical system such as a vehicle, sensor, helicopter, or Unmanned Aerial Vehicle (UAV) will comprise many subsystems with components and assemblies from many different suppliers. Such subsystems might vary from a mission computer to a multicomputing sensor processor, but all will require either the contractor or the original vendor to integrate, test, qualify, document, and maintain them. With increasing subsystem complexity, contractors are refocusing their technical skills on system-level technologies that will be of future value to their business rather than being, of necessity, embedded board-level computer subsystem integrators. These contractors are developing generic, portable applications that demonstrate a system's capability to customers and can quickly and easily migrate from development to deployed environment. This requires a higher level of service and support from their chosen COTS vendors.

Open standards support portability

There are two complementary paths to portability that include making extensive use of open standards and abstraction (or middleware). The government and end users strongly support the use of open standards available across a broad spectrum of applications, ranging from graphics and imaging to communications and networking. Open standards also include operating systems, operating system components, and APIs; development environments; compilers; design tools; and math and graphics libraries. Hardware open standards including VPX (VITA 46) and VPX-REDI (VITA 48) are well established and now also supported by OpenVPX (VITA 65), which clarifies concepts of architecture and interoperability. Middleware is often more closely tied to a specific hardware product, or to a range of COTS vendors' products, and industry standards such as Message Passing Interface (MPI) and Data Distribution Service (DDS) are gaining ground in this area. This middleware aims to create a common API allowing application modules to operate and communicate without reference to any hardware-specific details of the hosting embedded processors, fabrics, or networks.

Comprehensive and adaptable middleware forms an essential element of the subsystem integration effort, providing the integrator with a flexible model on which to base the communications design. This proves invaluable when, for example, concepts are taken from prototypes to representative hardware in the development laboratory and on to deployable hardware designed to meet all the project's environmental conditions. Prototyping and the development laboratory stages might use dissimilar host processors, while migration to deployable hardware becomes an opportunity for technology refresh, or even a review of suppliers. However, using open standards and abstraction is no guarantee of performance on the selected COTS vendors' products, making benchmarking or analysis-by-similarity essential steps in the process.

Performance specification

Some aspects of an integrated subsystem's performance are relatively easy for a contractor to specify to the COTS supplier: environmental, cooling, power dissipation, power characteristics, Electro-Magnetic Compatibility (EMC), functional requirements, memory size, I/O requirements, and so on. But much more difficult to specify is how the subsystem will perform when running the contractor's application and how the COTS vendor will prove the requirement is met. This becomes a joint responsibility, with the specification being developed as prototyping and testing proceed on the contractor's application. Once a configuration is established, it must be monitored for the impact of a COTS vendor's natural product line evolution, whether hardware, firmware, operating system, libraries, or drivers. Support for the same open standards must be maintained, and APIs to middleware or other embedded code such as system Built-in-Test (BIT) must have minimal future impact.

Integration of a subsystem requires more than the prerequisite range of services to configure, test, environmentally qualify, and document a set of COTS modules in a chassis. Experienced COTS vendors such as Curtiss-Wright Controls Embedded Computing (CWCEC) are able to offer complete, coherent solutions meeting customers' and end-users' objectives for use of open standards, portability, and longevity. Figure 1 illustrates an application-ready, VITA 46/48-based packaged subsystem for use in a ground-based radar application.

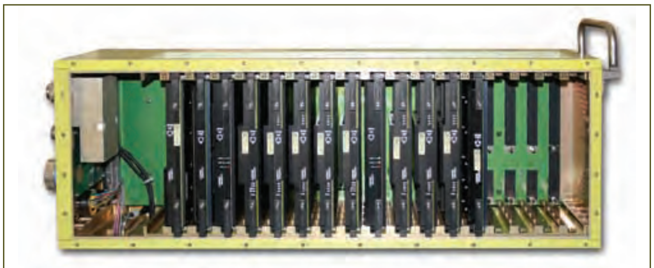

Figure 1 | Open standards COTS systems are deployed in a wide range of applications, such as a ground-based radar system.

Many contractors are looking for COTS vendors to provide ways to ease their integration headaches and ensure a level of continuity into the future. The growing complexity and capability of embedded computing products, based on standards such as VPX, will require COTS vendors to step up to the next level of subsystem integration: They must have the right products, services, middleware, and tools to assist in the rapid transition from concept to deployment.

To learn more, e-mail Steve at Steve.Edwards@curtisswright.com.


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By J. M. Schlesselman

Preserving legacy systems, by choice or necessity

Sometimes the best approach to preserving and extending aging military systems is the addition of modern protocol adapters. Consequently, new hardware and software come together to bring legacy equipment data into the network-centric world.

The U.S. Navy has an acute need to support legacy network systems while constantly adding new capabilities. This situation can span decades when today's new capability becomes tomorrow's legacy.

Some U.S. Navy programs are beginning to adopt computing plant technology insertion schedules that plan hardware upgrades every four years and software every two years. This approach ensures reasonably current technology, avoiding the life-cycle support problems of sourcing obsolete computer hardware for 10- to 20-year-old equipment.

But a problem remains: Not every ship system gets upgraded with the computing plant. How is today's technology integrated into older systems first developed in the '80s and '90s – without incurring unaffordable integration costs?

There are many possible solutions. One option is to rewrite and replace legacy software in the computing plant. Historically, this has proven very time consuming and costly. Other options include the development of bridging, routing, translating, or virtualization techniques. However, reprogrammable protocol adapters and Data Distribution Service (DDS) comprise the primary solutions.

Problem: Legacy sensors and weapons integration

The need to integrate existing systems with new capabilities is a common problem. For example, the U.S. Navy Cooperative Engagement Capability (CEC) program presents an integration challenge. CEC enables battle group ships and aircraft to share sensor (for instance, radar) track data, providing the entire battle group with a coherent, integrated air track picture.

CEC forms network-based tracks using existing sensors. However, the legacy system also creates a local track picture using the same sensors. A number of technical issues must be addressed to integrate both track managers: Sensor data provided to the CEC and the legacy system is neither time synchronized nor normalized. Additionally, the legacy system is not capable of immediately servicing requests from other applications that want to make use of sensor data. Sending raw sensor data to both systems results in track inconsistencies requiring resolution via additional algorithms.

Solution 1: Reprogrammable protocol adapters

Reprogrammable protocol adapters that translate legacy interface protocols (for example, NTDS-A/B/C/D/E) into current Internet Protocol-based DDS and Web Services (WS) protocols are easing the challenge of integrating old and new technologies. One such converter is Advanced Fusion Technologies' Open System Interface Adapter (OSIA).

OSIA abstracts the details of managing the legacy interface protocol, such as I/O chain management, from software applications running in the distributed computer plant. It also removes the computational burden of data formatting and input/output conversions. Instead of these cumbersome tasks, OSIA transfers data to software applications using standard Interface Design Language (IDL) formats. It enables applications to simply discover and subscribe to topic data via the DDS protocol using application-specific topic Quality of Service (QoS) parameters. Such protocol adapters also provide remote access to legacy data for browser-based applications via standard WS protocols. The resultant protocol adaptations lead to greatly simplified application integration.

Solution 2: Data Distribution Service

The other key old-and-new integration enabler is DDS software in the legacy computer distributed computing platform. DDS is the DoD-mandated standard for real-time publish/subscribe communications. Its chief benefit for legacy systems is that it facilitates an evolution from application-specific interfaces to data-centric programming. Data-centricity decouples information consumers (called "subscribers") from information producers (called "publishers"). This loose coupling between publishers and subscribers, complemented with fast and efficient bridging hardware, allows decades-old equipment to remain valuable in today's modern, IP-based systems.

The final result: Systems comprising old and new

The end result is a system that meets the competing needs of preserving the U.S. Navy's investment in legacy computing hardware while enabling the Navy's transition to an Open Architecture Computing Environment (OACE). Using OACE standard interfaces reduces costs by fostering competition, reuse, and interoperability. Bring reprogrammable protocol converter technologies into the picture, in addition to DDS, and costs decrease by allowing new and legacy systems to interoperate, eliminating the need to upgrade all systems in lockstep. This also reduces the cost of future technology insertions by having legacy equipment present the same interface as new equipment. This in turn allows procurement and R&D funding to be directed at the areas in which they will have the greatest impact.

J. M. Schlesselman *is director of aerospace and defense technologies at RTI. He has worked as a software developer, system integrator, and military officer. Joseph holds a Master of Science in Management Science and Engineering from Stanford University. He can be contacted at Joe.Schlesselman@rti.com.*

LCMR program continues to backtrack

Where did *that* come from? … In the heat of battle when mortar is being fired, locating and stopping its source is imperative to mission success – and to survival. Accordingly, the U.S. Army Communications-Electronics Command recently penned a $15.4 million contract with SRCTec for the first production order of the Lightweight Counter-Mortar Radar (LCMR) system's (V)3 (or third) variant. (The first two variants are widely deployed in combat operations.) LCMR – awarded a seat on the U.S. Army's Top Ten Inventions list – renders 360-degree coverage to facilitate location of mortar threats to in-theatre troops. Also known as AN/TPQ-48 (Figure 1), LCMR's *modus operandi* is to backtrack from the mortar shell to find its originating weapon's position. It is anticipated that the contract will be fulfilled by this September.

Figure 1 | LCMR technicians set up an AN/TPQ-48 for testing in the simulator's anechoic chamber. U.S. Army photo by Steve Grzezdinski.

Secure Internet: Impossible dream or pending reality?

While the *words* "secure" and "Internet" don't sound like they should even go in the same sentence, the *phrase* "secure Internet" sounds even more like an oxymoron. However, Lockheed Martin (LM) would probably beg to differ, having recently completed a successful Critical Design Review (CDR) of the Airborne, Maritime/Fixed Station Joint Tactical Radio System (AMF JTRS) – touted as "a secure, Internet-like tactical network." AMF JTRS aims to interconnect warfighters and the Global Information Grid (GIG) via its wideband networking, simplified upgrades, clarity of communications, and non-line-of-sight capabilities. Once 100 percent deployed, AMF JTRS is slated to connect more than 100 platforms and synchronize Navy, Air Force, and Army assets with soldiers in the field. The AMF JTRS team additionally comprises General Dynamics, BAE Systems, Raytheon, and Northrop Grumman.

Resources … knowledge … resources … knowledge?

In military (or even civilian) life, is it really those with the most toys who win – or is it those with the most knowledge? It's hard to say 100 percent of the time, but a recent $2 million contract for high-performance data storage and workstations for an airborne surveillance program suggest that the U.S. military is banking on school of thought #2. The contract stipulates that Z Microsystems provides its rack-mountable, ruggedized 2U ZXL2 workstations featuring hot-pluggable drives and slimline DVD-RW for the unidentified program. Optimized with a 550 W power supply and supporting AMD Opteron and Intel Core 2 Duo boards, the ZXL2 is also compatible with PCIe graphics cards. Z Microsystems will additionally supply its rugged removable storage module, dubbed the "TranzPak 7," providing a single docking station and up to 2 TB storage. TranzPak 7's removable drive format enables operators to easily remove or plug in whole operating systems at any locale.

UAS controller flies from commercial to military side

Often the most sought-after embedded technology wares are those that can go from commercial use to military adoption with minimal (or no) design adjustments. Accordingly, a recent inaugural "proof of concept" flight demo was held by AAI Corporation and GE Aviation in cooperation with the U.S. Army and Federal Aviation Administration (FAA). The demonstration's goal was to show that GE's Flight Management System (FMS), certified for commercial manned aircraft applications, is a safe mechanism with which existing Unmanned Aircraft Systems (UASs) could also be controlled by the U.S. Armed Forces. The initial 45-minute demo flight included vertical and lateral control of the Shadow 200 UAS via FMS. Meanwhile, GE's flight management systems can be found in the P-8A Poseidon (Figure 2), the C-130 and E-4, Boeing 767 tanker, and many more.

Figure 2 | P-8A Poseidon, photo courtesy of Boeing

Caught in the middle of NASA technology

While the phrase "caught in the middle" typically carries a negative connotation, the center of things is a common locale for modern middleware; however, middleware aims to solve, not perpetuate, issues. Case in point: NASA's Human-Robotic Systems Project, which includes four very different robots slated to use one common data system. The enabler: Real-Time Innovations (RTI) Data Distribution Service (DDS) middleware. The "players" include Jet Propulsion Lab's ATHLETE, a six-limbed, large-stature, large payload-carrying robot operating in terrains such as rocky areas and steep slopes; the Lunar Electric Rover (LER) depicted in Figure 3, created by Johnson Space Center and destined to transport astronauts on Mars or the moon; K10, designed by NASA's Ames Research Center, which operates either independently or via human control as it utilizes a suite of laser scanners and cameras; and Lunar Surface Manipulator System (LSMS), a crane-like robot in development at Langley Research Center and anticipated to assist with loading and assembly tasks on planetary surfaces. The integral DDS middleware will facilitate a single common communications architecture amongst all four robots, providing high-speed communications while reducing ground staffing, simplifying equipment, and eliminating duplicate testing of the robots.

Figure 3 | Lunar Electric Rover (LER), created by Johnson Space Center, is destined to transport astronauts on Mars or the moon. Photo by NASA/Regan Geeseman

U.S. DoD entity turns to social media

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Hardly a day goes by without the mention of social media. It's "virtually" everywhere and seemingly used by everyone … almost, anyway: individuals and increasingly by businesses and other entities. Recently, the U.S. DoD's health-care provider, Tricare, even boarded the social media train. The reason: to provide Tricare's service recipients – uniformed service members and their families – the opportunity to weigh in on health-care concerns and perhaps influence policy decisions. In a statement to the media, Navy Rear Adm. Christine Hunter, who serves as Tricare Management Activity deputy director, said, "Social media is changing the way we communicate. These powerful tools give us an opportunity to join the conversation surrounding Tricare and military health." Accordingly, Tricare has active accounts on Flickr, YouTube, Twitter, and Facebook. Tricare will also seek beneficiary preferences regarding its new media center Web page, slated for a March launch, by checking responses on its Facebook and Twitter accounts beforehand.

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Figure 4 | The USS Missouri recently made the 2-mile voyage home to Pearl Harbor's Battleship Row's Pier Foxtrot-5, where its new memorial recently opened. U.S. Navy photo

"Mighty Mo" returns home

World War II history buffs will recall that the attack on the USS Arizona in Pearl Harbor began the "day of infamy," and that the USS Missouri was later the locale of Japan's surrender in Tokyo Bay (Figure 4). The good news: "Mighty Mo," after having served faithfully in three wars and five decades now gets her due: The USS Missouri recently made the 2-mile voyage home – after a multimillion-dollar, 12-week drydocking – to Pearl Harbor's Battleship Row's Pier Foxtrot-5, where she will reside in close proximity to the also-resting USS Arizona Memorial. After decommissioning, USS Missouri was donated to the USS Missouri Memorial Association, which recently opened the new Battleship Missouri Memorial at the ship's Pier Foxtrot-5 Pearl Harbor home.

Chinook upgrade validates Newton's third law

Sir Isaac Newton's third law of motion states that for every action, there is an equal and opposite reaction. Proving the centuries-old axiom is BAE Systems, which recently outfitted the military's CH-47D Chinook with modern fare: the Advanced Threat Infrared Countermeasures (ATIRCM) system. (Though Newton couldn't have predicted helicopters let alone countermeasures, his theory is, nonetheless, validated.) The laser-based ATIRCM's mission is to protect helicopters from missile attacks via its directable countermeasures system. Though the CH-47D was first deployed in 1982 and in production through 1994, it is still used today in the global war on terror (Figure 5) thanks to modernization efforts such as ATIRCM and others.

Figure 5 | Though the CH-47D was first deployed in 1982 and in production through 1994, it is still used today in the global war on terror. U.S. Army photo by Lance Cpl. Ryan Rholes

Foresight beats out hindsight … but only in the case of model-based design

Interview with Dr. Jon Friedman, The MathWorks

EDITOR'S NOTE

It doesn't matter which type of ware is being viewed. The purpose of modeling is always the same: The visionary gets to see the possibilities – before any investment is made. And the same applies to military embedded technology, according to The MathWorks' Dr. Jon Friedman: Rather than use the same old Line Replaceable Unit (LRU) approach where snafus are found near the end of the design road, model based design enables engineers to "virtually" see the end from the beginning – and eliminate those costly late-game redesigns. We also found out some of the company's hot new focal points and why they are – or will be – important to the defense industry.

MIL EMBEDDED: ***Your products run the gamut across use in systems engineering, algorithm development, code analysis, and test and measurement. Can you briefly summarize your focus areas for defense and aerospace markets?***

FRIEDMAN: The MathWorks supports engineers in the aerospace and defense markets across a wide range of applications including aircraft control systems, land systems, and spacecraft as well as advanced communication systems and new sensor and signal processing applications. These focal points are facilitated primarily with two platform products: MATLAB and Simulink.

MIL EMBEDDED: ***OK, can you tell us a little about MATLAB first, then Simulink?***

FRIEDMAN: Certainly. MATLAB is a platform for technical computing. To put the term "technical computing" into context, think about engineering activities like data analysis and visualization, test data and signal creation/synthesis, algorithm development/synthesis, and algorithm testing/analysis. Engineers developing sensors to capture images need to characterize and calibrate the sensor before they can create the algorithms that use the images for intelligence, surveillance, or reconnaissance work. To accomplish this task, they collect and analyze data from the sensor. They will then build a mathematical model of the sensor's dynamics. Using this model, the engineers can then determine the optimal calibration for the sensor.

The other product, Simulink, is the platform for model-based design. In the past, using a traditional Line Replaceable Unit (LRU) design process, engineers gather requirements from several sources, which are combined to create a paper specification and often take up numerous binders on an engineer's desk. An acceptable design is eventually achieved, then handed off to another team that performs verification and validation testing. Because testing occurs at the end of the design process, errors that are introduced throughout the design process are often found late, making them expensive to fix. In contrast, model-based design such as that offered by Simulink, begins with the creation of an executable specification that can be linked to the original requirements, providing two-way traceability between the design and the requirements.

> "With model-based design, development teams use the same tool platform to incrementally design and test, building from requirements definition all the way to integration testing."

MIL EMBEDDED: ***Though many systems engineers recognize the benefits offered by MATLAB and Simulink, you're also encouraging more software programmers to use the tools and underlying data. What are the use cases and benefits?***

FRIEDMAN: In the development of complex systems, engineers often focus on one specific area, such as controls algorithms, communications designs, or software programming. The outputs of these groups must ultimately meet the same requirements. However, when these groups are operating in completely different environments, there are many opportunities for designs to diverge. Model-based design such as that offered by MATLAB and Simulink enables engineers to collaborate early in the development cycle and to reuse models in different stages of design. Not only is the end design better optimized for functionality and performance, early-stage design iterations are also significantly less expensive than those made after code has been completed.

MIL EMBEDDED: ***How can your modeling (MATLAB and Simulink) and code analysis/verification (PolySpace) products work together for development teams?***

FRIEDMAN: Model-based design bridges multiple disciplines, from controls to communications and from system engineering to testing. This enables teams to easily share requirements, models, data, and test cases. With model-based design, development teams use the same tool platform to incrementally design and test, building from requirements definition all the way to integration testing. For example, the team can model requirements and functional design in MATLAB and Simulink, produce code using Real-Time Workshop Embedded Coder, and test the code using PolySpace and Simulink verification and validation tools.

MIL EMBEDDED: ***Can you share an example of a current defense program where this more integrated development approach is making a big difference, and highlight the before and after?***

FRIEDMAN: In 2004, BAE Systems was tasked with developing a military standard (MIL-STD-188-165A) satellite communications waveform for implementation in a Command, Control, Communications, Computers, Intelligence, Surveillance, and Reconnaissance (C4ISR) radio. At the same time, BAE Systems sought to evaluate a new design flow for reducing development time. Working together, BAE and Xilinx ran two projects in parallel, one using BAE Systems' traditional design flow, which relied on hand-coding VHDL. The other project utilized a model-based design flow involving automatic code generation using The MathWorks and Xilinx tools. To ensure a fair comparison, each effort used an equivalent set of IP cores.

MIL EMBEDDED: ***So what were the results of the two differing design flow methodologies?***

FRIEDMAN: Dr. David Haessig, manager of Waveform Products at BAE Systems, summed it up best when he said, "With the model-based approach, we developed a common model of the waveform, which was used for performance simulation, operational debugging, and code generation. As a result, we demonstrated more than a 10-to-1 reduction in the time to develop the signal processing chain of a Software-Defined Radio. This really illustrates the potential for improving productivity in SDR applications."

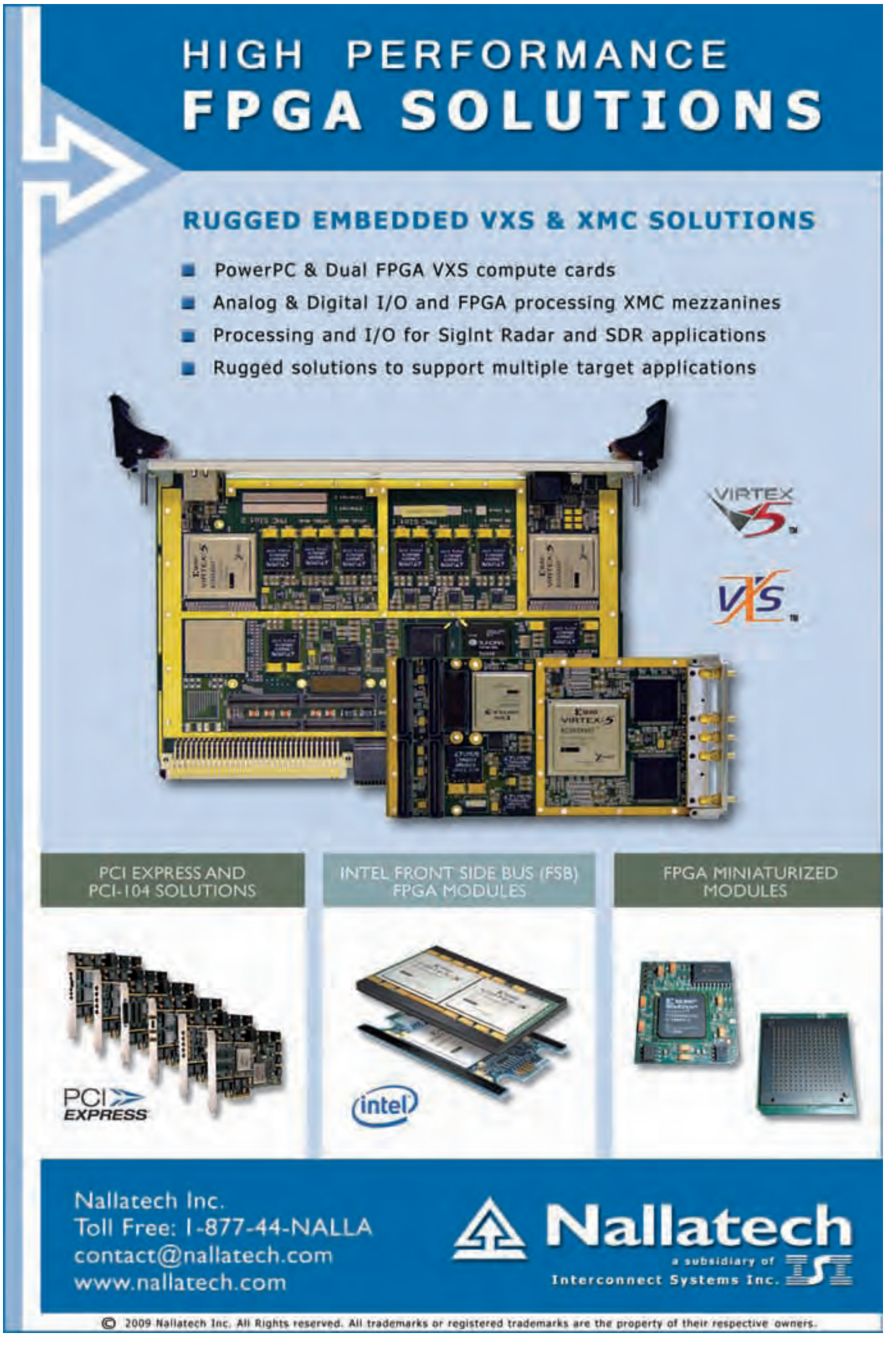
The most impactful result was a reduction of more than 4-to-1 in overall project time including hardware integration and lab testing. Also, with model-based design, the Simulink model was directly connected to the resulting code, which forced the developer to capture all of the required waveform details in the model leading to earlier discovery. This meant bugs were discovered and removed early in the design flow – at the modeling stage, not later at the VHDL behavioral testing stage where they can be difficult and time-consuming to fix. Another big advantage with Simulink and System Generator was that the necessary clocking signals were generated automatically, and components were connected easily, reducing the need to study the data sheet for details concerning control, timing, and other options.

MIL EMBEDDED: ***What are some other hot areas for The MathWorks right now, and why are they important to the defense industry's future?***

FRIEDMAN: I'd have to say avionics safety standards and also sensor systems.

Regarding avionics safety standards, all commercial aircraft software and electronics must be certified as compliant with the DO-178B and DO-254 safety specifications to have authority to fly in commercial airspace. Many defense suppliers are also required to certify military systems or follow processes compliant to these standards for applications such as Unmanned Aerial Vehicles (UAVs). Estimates predict that conformance to DO-178B adds 50 to 200 percent to software development costs. However, model-based design is one way to reduce costs by integrating verification activities earlier in the design process to ensure conformance to standards. These tools can aid designers in four key areas: traceability, requirements validation, verification, and conformance.

As far as sensor systems are concerned, as you know, they are at the heart of many new defense programs and upgrades to existing military equipment. Unmanned systems rely on video and infrared sensors for navigation and tracking. Anti-IED technologies often employ a suite of sensors to help detect threats. These sensor systems can vary in terms of the types of signals being analyzed (RF, optical, infrared, or acoustic), the types of analysis being performed (spectral or object detection), and the platforms upon which they run (DSP, FPGA, or ASIC). However, most development activities fall into three categories: understanding and characterizing the sensor itself, processing data read from the sensor unit, and performing higher-level analysis. So we design our tools to help engineers throughout this process.



MIL EMBEDDED: ***Where is the next frontier for The MathWorks in developing tools for defense software development teams?***

FRIEDMAN: One area of focus for the company is continuing to build capabilities to support verification and validation activities. Using MATLAB and Simulink to design and verify early in the process is well established. The MathWorks is focusing on developing tools to help designers use models to help them in the other verification and validation tasks with which they are faced. Examples include leveraging parallel computing capabilities for executing large numbers of simulations, complementing simulation with property proving on models and code, and using formal analysis to help in automatic test case generation.

Dr. Jon Friedman *is the aerospace & defense and automotive industry marketing manager at The MathWorks. Prior to joining The MathWorks, he worked at Ford Motor Company, where he held positions ranging from software development research to electrical systems product development. Jon has also worked as an independent consultant on projects for Delphi, General Motors, Chrysler, and the U.S. Army Tank-automotive and Armaments Command (TACOM). He holds a B.S.E., M.S.E., and Ph.D. in Aerospace Engineering as well as a Masters in Business Administration, all from the University of Michigan. He can be reached at jon.friedman@mathworks.com.*

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U.S. Air Force photo/Airman 1st Class Corey Hook

Intel Architecture: All set for high-performance military embedded signal processing applications

By Peter Carlston, Intel Corporation, and
Ian Stalker, Curtiss-Wright Controls Embedded Computing

The latest Intel Core i7 dual-core processors provide users with an alternative to Power Architecture processors for DSP applications.

Historically, processors from the PowerPC family, now known as Power Architecture processors, have been the dominant choice for implementing Digital Signal Processing (DSP) in high-performance embedded military applications that take advantage of open-system COTS products. Today, however, beginning with Intel Core i7 dual-core processors, low-power, high-performance Intel Architecture processor technology provides, for the first time, an attractive alternative for designers of DSP engines for the rugged deployed COTS signal processing space.

Signal processing evolution

Since the 1990s, processors from the PowerPC family (also known as Power Architecture) and their AltiVec floating-point vector math unit have been the dominant choice for open-system COTS boards used in high-performance embedded military DSP applications. These applications include radar, signals intelligence, sonar, and image processing. Previously, such systems were largely implemented with specialized processors such as the Intel i860, the Texas Instruments 320C40, and the Analog Devices SHARC. These processors were popular because of their floating-point performance.

In the late 1990s, the COTS market turned to the PowerPC processors developed by an alliance of Apple, IBM, and Motorola (later Freescale) and intended for personal computers. The resultant high-performance microprocessor was based on a RISC architecture, but it was the introduction of the AltiVec instruction unit in the Motorola PowerPC 7400 ("G4") that changed the signal processing landscape.

Signal processing experts were quick to recognize that the floating-point capable AltiVec unit could greatly accelerate the inner-loop processing found in common functions such as Fast Fourier Transforms (FFTs). AltiVec's ability to perform up to four simultaneous floating-point multiplies and additions was, at the time, revolutionary.

FFT performance on an Intel Core i7 processor

One of the most common signal processing algorithms is the FFT. The FFT implementation shown in Figure 1 is a version that is included in the Intel Performance Primitive (IPP) library.

This example uses 32-bit single-precision complex floating-point samples. The FFT is implemented for different sizes, and the number of cycles per sample has been measured. The results were profiled on an Intel Core i7 processor running at 2.67 GHz. The processor has four cores, but these tests only use a single thread. (Note that the Intel Core i7 processor utilizes the Intel Microarchitecture in a 32 nm fabrication process.)

The IPP implementation of an N point FFT uses a complex multiplication taking six operations (2MUL & 2ADD) and a complex addition taking two operations (2ADD) for each point. Since a MUL takes four operations, this amounts to $8N.\log_2 N$ floating-point operations (FLOPS). By calculating the number of FLOPS per cycle, the sustained GigaFLOP performance can be derived. A single core is capable of 20 to 30 GFLOPS for FFT execution, which is up to more than 90 percent of theoretical capability.

In the meantime, Intel continued to develop the floating-point capability of its own processors, including a vector-processing unit generically known as Streaming SIMD Extensions (SSEs), first introduced in the Pentium III processor. Intel has continually added features and new instructions, culminating in the current implementation, SSE 4.2.

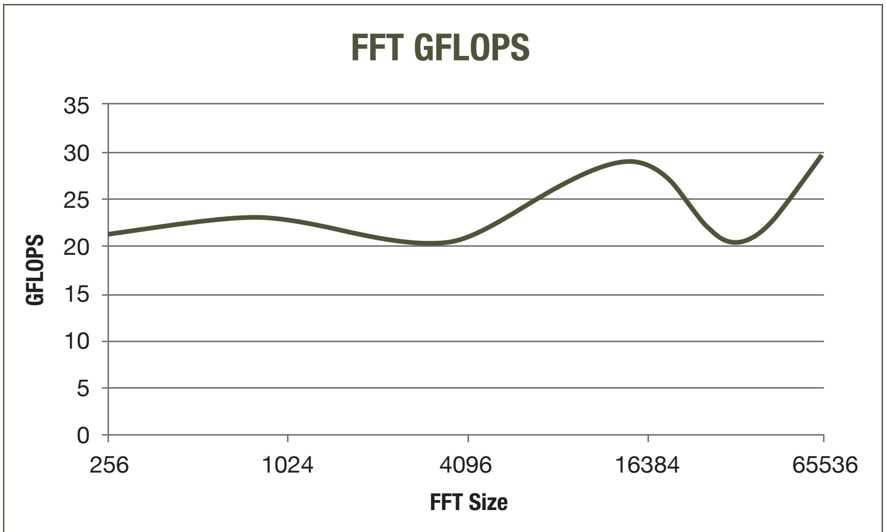

Figure 1 | FFT performance in GFLOPS

Like AltiVec, SSE is a 128-bit wide processing unit, capable of simultaneously operating on four 32-bit floating-point values. SSE also features support for double-precision floating point, a feature that was never included in AltiVec. (Note that Freescale has decided not to include the AltiVec unit in its latest high-performance processor, the QorIQ P4080. The P4080, announced last year, is an excellent CPU for single board computer designs because of its eight cores, integrated memory controllers, and Serial RapidIO interface; however, it features a regular floating-point capability that is not the vector processor type required to attain the floating-point performance needed for signal processing applications.) In multicore Intel processors, each core has its own SSE unit, so the raw floating-point performance scales with the number of cores.

Additionally, Intel x86 processors are classic CISC processors. Successive generations of Intel processors continue to dispatch more instructions per clock. Since many more instructions are executed per clock cycle and the code density is higher, Intel processors can perform more than twice the useful work per clock cycle as a Freescale RISC processor. As a result, beginning with Intel Core i7 dual-core processors, the low-power, high-performance advantages of the Intel Architecture processor technology can be used for the first time to design products such as DSP engines for the rugged deployed COTS signal processing space.

Intel Architecture meets signal processing performance needs

The latest generations of Intel Architecture processors are produced on 45 nm and 32 nm process technologies and are based on the Intel Microarchitecture, which includes many features that suit high performance and power-efficient execution of signal processing workloads.

To support high instruction throughput, the Intel Microarchitecture contains a sophisticated memory subsystem. In a quad-core processor, each core contains a first-level instruction cache (32 KB 4-way), a first-level data cache (32 KB 8-way), a second-level unified cache (256 KB 8-way), and a third-level cache of up to 8 MB 16-way that is shared among all the processor cores. With 2 or 3 DDR3 memory controllers, the processor can provide a peak memory bandwidth of 17.1 or 25.6 GBps. This high-throughput capability is required to support the multi-gigabit rates for the processing of the sample streams in military signal processing applications such as radar.

Support for the efficient implementation of high-throughput signal processing is based on SSE instructions, which are extensions to the standard Intel Instruction Set Architecture (ISA). Including the latest generation, SSE 4.2, there are more than 300 SSE instructions. SSE operations work from a set of 16 128-bit wide XMMx registers, capable of simultaneous operation on four packed floating-point values, as well as other formats.

Effective implementation of signal processing algorithms requires efficient use of all resources on the processor platform, so the ability to parallelize algorithms across multiple cores in a linear manner is essential. Parallelized scaling across the multiple cores of an Intel

Microarchitecture-based platform can be executed for common operations used in signal processing such as complex multiplication, or for more computationally intense algorithms. A threading model can be used to implement the complex multiplication algorithm with parallel execution.

A single quad-core processor Intel Core i7 platform can be used to execute the complex floating-point multiplications. The results depicted in Figure 2 show the expected linear performance scaling from one to four threads, as additional cores and SSE vector units are employed in the algorithm. The eight-thread case demonstrates that additional efficiency can be obtained from the hyper-threading feature of the cores, even though the floating-point calculation resources of the core remain the same between the four-thread and eight-thread case.

Curtiss-Wright's first multiprocessor DSP board products will be based on the recently announced dual-core Intel Core i7 610e.

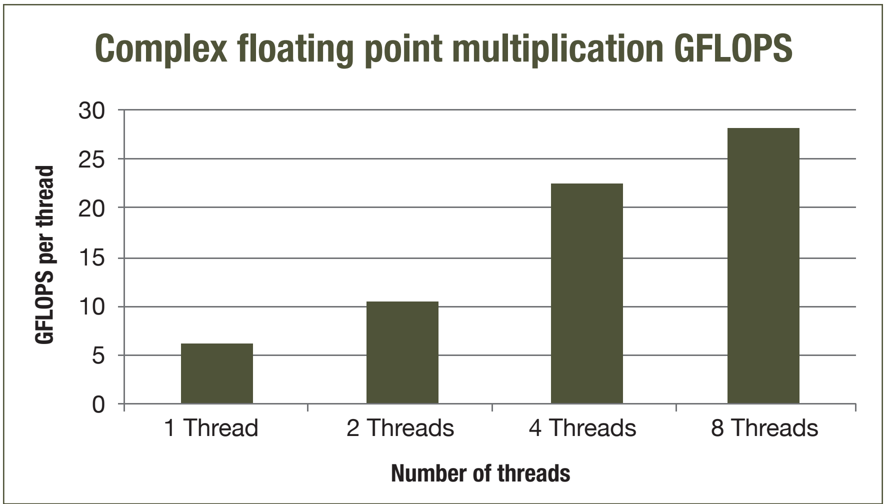

Figure 2 | FFT performance: GFLOPS versus number of threads

The first two products based on the Intel Microarchitecture are the CHAMP-AV5 6U VME64x DSP engine and the SVME/DMV-1905 SBC. Additionally, an Intel Core i7 architecture dual-core processor OpenVPX Ready (VITA 65) variant of the CHAMP-AV5 DSP, the CHAMP-AV7, is scheduled for release in the summer of 2010. Using two 2.53 GHz dual-core Intel Core i7 processors, the CHAMP-AV5 delivers performance rated up to 81 GFLOPS. With 4 MB of cache and two hardware threads per core, the Core i7 can process larger vectors at peak rates significantly greater than was possible with previous AltiVec-based systems.

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Top technologies for the warfighter

By Chris A. Ciufo, Editor

Our third-annual look at commercial technologies coming to a battlefield near you.

Mooly Eden, Corporate Vice President, General Manager, PC Client Group at Intel Corporation holds early-release silicon of Intel's Core i7 mobile processor and chipset, which was formally announced in January 2010.

What started out as "This year's top trends affecting the military" in the January/February 2007 Crosshairs Editorial column of this magazine (see article at www.mil-embedded.com/articles/id/?2497) has morphed into an annual prediction of winning technologies most likely to be designed into defense programs. This year, *Military Embedded Systems* editors came up with independent lists, compared notes, and whittled it down to our top five technologies and our favorite industry enabler. The list was strongly influenced by the Consumer Electronics Show (CES) in Las Vegas, showcasing the best embedded civilian, consumer, and commercial technologies. And why not? That's what COTS is all about. Here's this year's list, banded into three broad categories affecting Aerospace and Defense (A&D).

Intel Core Technology CPUs

Like shuttle launches into space, everyone's gotten so used to AMD and Intel CPU product announcements that they've become sort of ho-hum. As one who follows the Intel roadmaps carefully (refer to "Tasty alphabet soup from the Intel Developer Forum" www.smallformfactors.com/articles/id/?4331), the nuances from Pentium III to 4 to M and finally Core 2 are interesting in their constant incremental improvements. Sure, Intel's MMX instructions set the stage for the multimedia phenomenon back with the PIII and the migration to built-in graphics controllers in chipsets. As well, the company's high K dielectric patents allowed reduced transistor gate thicknesses without punch-through, keeping Moore's Law and technology marching forward. But the 33 Core Technology CPUs, chipsets, and wireless peripherals announced this January seemed to be the culmination of 10 years of Intel's best technology flawlessly timed to coincide with a number of converging market factors[1].

The Core family consists of Core i7, Core i5, and Core i3 CPUs broken into mobile, desktop, embedded, and wireless subcategories. There are 29 CPUs and 4 Centrino wireless devices; the embedded lineup is shown in Table 1. Not unlike BMW nomenclature, Intel says the flavors represent "good, better, best" versions of the CPUs with enhanced features (but not necessarily clock frequency). Notable technology "firsts" are Intel's $7 billion investment that resulted in leading-edge, high-volume 32 nm devices all released to mass production simultaneously. Think about the logistics of that for a moment. As well, the Core family introduces a number of new features, including bringing the graphics controller on-chip in some versions, ECC and higher-performance DDR3 SDRAMs (versus DDR2), and a new feature called Turbo Boost. Any one of these achievements is incremental: Taken together, they've rocked the market.

Turbo Boost, for instance, dynamically adjusts the multicore frequency (up to four cores) in Core i7 and Core i5 devices running within Thermal Design Power (TDP) limits. Fully automatic and enabled by the system BIOS, mobile, desktop, and extreme processors will run at faster frequencies (in multiples of 133 MHz) when an application demands it and when excess bandwidth exists on available cores. Available for both single- and multithreaded applications, the technology hardly seems revolutionary, but Intel benchmark data shows that a sole multicore Core i7 or i5 processor running in Turbo Boost mode can often obviate the need for additional CPUs in a system. This lowers overall Size, Weight, and Power (SWaP) and saves costs in demanding mobile, desktop, and server applications.

As of the end of January, nearly every COTS SBC vendor tracked by *Military Embedded Systems* has announced Core Technology products, including Congatec, Curtiss-Wright Controls Embedded Computing (CWCEC), Concurrent Computing, GE Intelligent Platforms, Extreme Engineering, Hybricon, Kontron, Mercury Computer, One Stop Systems, Tracewell, and numerous others. (We'll do a roundup of COTS offerings in the March/April issue.) To have so many small form factor, COM, VME, and custom system vendors revamp their product lines simultaneously to a new processor is

Intel Core embedded line-up

Processor number	Base clock speed (GHz)	Turbo frequency (GHz)	Cores/Threads	Thermal design power	Error correcting code
Intel Core i7-620M	2.66	Up to 3.33 GHz	2/4	35 W	No
Intel Core i7-610E	2.53	Up to 3.20 GHz	2/4	35 W	Yes
Intel Core i7-620LE	2.0	Up to 2.80 GHz	2/4	25 W	Yes
Intel Core i7-620UE	1.06	Up to 2.13 GHz	2/4	18 W	Yes
Intel Core i5-520M	2.4	Up to 2.93 GHz	2/4	35 W	No
Intel Core i5-520E	2.4	Up to 2.93 GHz	2/4	35 W	Yes
Intel Core i5-660	3.33	Up to 3.60 GHz	2/4	73 W	Yes
Intel Core i3-540	3.06	N/A	2/4	73 W	Yes
Intel Core i7-860	2.8	Up to 3.46 GHz	4/8	95 W	No
Intel Core i5-750	2.66	Up to 3.20 GHz	4/4	95 W	No
Intel Xeon X3450	2.66	Up to 3.20 GHz	4/8	95 W	Yes
Intel Xeon X3430	2.4	Up to 2.80 GHz	4/4	95 W	Yes

Table 1 | Intel's embedded Core processors showing i7, i5, i3, and Xeon versions. The i3 to i7 are sort of like "good, better, best."

[1] Factors are: always-on Internet connectivity, long battery-life portability, small-screen high-quality multimedia, increased privacy and data security on all devices – portable or not, aging populations and how to care for them, and worldwide growing demand for access to the Internet.

unheard of. The last time I saw this kind of industry sea change was from the Motorola 68020/40 to the PowerPC (PPC).

The Intel devices not only offer amazing general-purpose and graphics capabilities, they do a pretty good job of signal processing (refer to article on page 42). Look for the PowerPC and its AltiVec vector processor to fall out of favor in signal processing; I'd even expect to see EOL notices on some PPC products as Freescale focuses more on Ethernet-equipped SoC-based PowerPC devices instead of CPUs. With on-chip 3D graphics in Core CPUs, there will be less need for ATI or NVIDIA GPUs except in ultra-high-end plug-in devices – but that's not the sweet spot of the market anymore.

E-books, Android, iPhone … and iPad

Intel popularized the term Mobile Internet Devices or *MIDs* when it claimed in 2008 that there would be 15 billion MIDs within a few short years. One new category of MID from CES was manifested in the endless parade of e-book readers from Samsung, Interead, ONN, and a pile of other companies you might not have heard of[2]. From a consumer perspective, e-books might replace books, allow one to carry multiple documents to read on airplanes or in coffee shops, and provide a larger screen from which to send emails than an iPhone-sized LCD. E-book readers by definition have to marry screen readability with sunlight viewing and battery life. As a technology class, they are a proving ground for SWaP, highly integrated System-on Chip (SoC) devices with wireless networking (often based upon ARM Cortex IP or Intel Atom), and new crisper LCDs that maintain their image even when virtually powered off. Some, like the Alex, have an LCD and e-ink grayscale screen.

In the defense markets, beyond the general trend toward SWaP, all programs require embedded training, logistics management through depot sourcing, and maintenance manuals. E-book readers could be applied at all stages of a production program: from initial training, through maintenance, and out to the tip of the spear with warfighters themselves

“… The iPhone – and its just-announced at press time iPad big brother – are probably the best examples of pure civilian technology that is benefitting the warfighter.”

using them to replace bulky C4I laptops now lugged in knapsacks.

Yet it's Google's Android operating system that is perhaps the more exciting technology, acting as a catalyst that's spawning new ideas while making possible rapid time-to-market of new MIDs like Barnes & Noble's nook, Alex's twin-screen e-book, or Motorola's DROID smartphone. As of the end of 2009, Internet sites like engadget and Wikipedia were tracking nearly 50 Android devices. Traditional tech companies such as Mentor Graphics are extending their EDA tool suites into Android development. Mentor purchased Embedded Alley Solutions in an effort to capitalize on how Android's Linux-based, open-source OS and middleware are likely to crack wide-open the stranglehold of proprietary software. Even companies like MontaVista with their Linux 6 are banking on Android by offering hardware drivers, an application stack, and user interface options.

Lastly, the iPhone – and its just-announced at press time iPad big brother – are probably the best examples of pure civilian technology that is benefitting the warfighter. In September 2009, Apple disclosed that there were 85,000 apps available for the device; by November, *Wired* magazine reported the number exceeded 100,000. Today, that number is 140,000. The user-friendliness of the iPhone, despite being chained solely to AT&T's 3G network, makes it literally the next-generation computer for the entire world. Last year's "cheap laptop" netbook is doomed, says Apple's Steve Jobs[3]. Already DoD personnel use iPhones to read "sit rep" reports while communicating with operations centers. Video is easily shared, and AES encryption plus memory-resident databases from companies like McObject make the iPhone – and potentially the larger iPad –

[2] The e-book category is not really "new." The first high-volume production, dedicated e-book was the Rocket eBook from Nuvomedia, around 1999. Fun fact: Some of the founders of that company went on to found Tesla Motors, manufacturers of the much heralded all-electric sports car available today.

[3] This writer briefly owned a netbook last year. Loved the price and the build quality of the ASUS Eee PC; hated the diminutive clamshell form factor. The screen should've folded back flat, like a Toshiba M205 TabletPC.

New Aitech NightHawk RCU™ Controller:





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Photography Courtesy of Lockheed Martin

a must-have for locations with AT&T coverage. Admittedly, that's not Iran nor Afghanistan, but iPhone-envy will surely encourage more iPhone-like, Android-based, purpose-built DoD platforms.

Open standards

Our last key technology for the warfighter isn't a technology at all: It's the impetus for a collection of products. Indeed, the era of COTS paved the way to breaking "stovepipe" defense systems supplied cradle-to-grave by one contracting team. But custom off-the-shelf software, boards, and systems can still leave the government beholden to a single supplier – albeit not the same prime contractor as before. Open standards, such as ANSI/VITA-1, bring nearly 30 VME companies in competition for military programs, with guaranteed interoperability at predefined abstraction layers. VITA's latest open standard – OpenVPX, called VITA 65 – switches from a parallel backplane to hundreds of serial pairs for nearly 5 Gbps data rates. Twenty-eight companies have announced plans to build or use OpenVPX. Additionally, in 2009, eight VITA specifications achieved ANSI ratification, signaling their official interoperability status.

Other board-level standards such as PICMG's AdvancedTCA rack-mount standard are migrating from telecom installations to mostly benign, deployed defense racks in trailers, TOCs, and tents. Server and datacom companies including RadiSys and Emerson are converting their rugged NEMA-rated hardware systems to MIL-HBK-217 specs – another example of COTS open standards benefitting A&D by bringing server-class muscle to the battlefield.

In software, Carrier Grade Linux brings High Availability (HA) to these rack-mount systems, along with the Service Availability Forum's OpenSAF HA middleware. SA Forum specs for the application interface, hardware platform, and others are being implemented by COTS companies such as GoAhead Software. Interoperable network management software is also being opened up with standards for SNMP and NETCONF, from companies such as GoAhead and Tail-f Systems. Here too, the availability of standards to which any company can create software is giving a real edge to battlefield networks and directly benefitting the warfighter in programs such as the Navy's Aegis/Common Processing System.

Finally, one of the most unusual open standard specs might be the artificial intelligence Resource Description Framework (RDF). Started as a way of representing Web pages and data on the Internet, RDF works with semantic fusion and Natural Language Processing to convert massive amounts of seemingly unrelated data events into searchable (and most importantly), "relatable" chunks that can be assembled in new ways. Companies like Modus Operandi have won DARPA contracts to take open source data and use it for tactical exploitation. Think about mining blog postings on a bad actor's website and correlating them with a passport database, or even debit card transactions. RDF allows creating reconnaissance software that promises "never before" tactical information – and thus, another benefit to the warfighter.

U.S. Navy photo by Mass Communication Specialist 2nd Class John Philip Wagner Jr.

The systems engineering relationship between qualification, Environmental Stress Screening (ESS), and reliability

By James A. Robles

The systems engineering relationship between qualification, ESS, and reliability is often poorly understood. As a consequence, resources are often expended on efforts that degrade inherent hardware reliability and vitiate reliability predictions. James expounds upon this relationship and how proper application enhances inherent reliability and supports credible reliability predictions.

There is a problem with the reliability of recently fielded systems: Department of Defense concerns have been widely reported. This is not a COTS versus "custom or military specification design" issue. The focus is on program management and best practices.

This focus on processes and practices is a positive development; however, it is essential that we get the "content" right. Two areas where there seems to be widespread failure to do so are the definition of endurance/durability/life environments, and the application of ESS. Additionally, the reliability prediction process has its own limitations; however, program managers can avoid these pitfalls with some careful consideration.

Endurance/Durability/Life environments

The "bathtub curve," shown in Figure 1, can be used to describe a range of phenomena including human death rates as a function of age, and electronic failure rates as a function of time. The "infant mortality" portion of the curve is the initial section for which the failure (death) rate of electronics decreases with time (age). This higher initial failure rate is due to latent manufacturing defects. ESS, comprising random vibration and temperature cycling, is used to precipitate these defects as failures so that they can be repaired.

The "constant failure rate" portion of the curve is the section after infant mortality defects have been eliminated. But before wearout begins to occur, failures are "random." This is the period for which constant failure rate statistical prediction techniques (MIL-HDBK-217, VITA 51.1, and so on) have some validity.

The "wearout" portion of the curve is the last section where the failure rate increases substantially due to metal fatigue. Durability/endurance/life verification (analysis

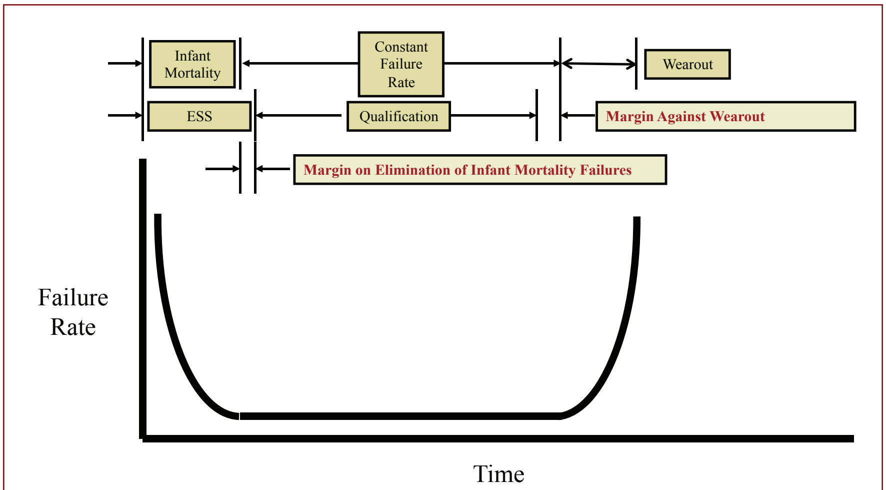

Figure 1 | The bathtub curve can be used to describe a range of phenomena including human death rates as a function of age, and electronic failure rates as a function of time.

and/or test) during item qualification is intended to demonstrate that wearout will not occur during the planned life of the item.

Limitations of the reliability prediction process

MIL-HDBK-217 (as do most similar analysis techniques) relies on a number of assumptions, two of which are germane here:

1. Infant mortality failures have been eliminated by good process control, or screened out by an effective ESS program that consumes a relatively small percentage of "demonstrated life."
2. The period of performance after ESS is within the "demonstrated life" of the item, so that "wearout" failures will not occur.

Selecting the applicable MIL-HDBK-217 "PiE-factor" (the adjustment factor for severity of environment) will not remotely compensate for the failure to adequately specify durability environments. The "PiE-factor" ratios assume, as does everything in the MIL-HDBK-217 methodology, that durability has been demonstrated and that the item is in the "constant failure rate" portion of the bathtub curve. They do not account for limited life due to "wearout."

The salient contributors to equipment endurance/durability/life environments are vibration and temperature cycling. The deleterious effects of these environments are widely understood, and have been thoroughly investigated in a number of venues.

The Bolton Memorandum and ANSI/GEIA-STD-009 both confirm the need to address the fatigue aspects of both thermal and vibration fatigue. Ideally the durability environments should be derived from the item's planned usage.

The temperature cycling fatigue environment is usually caused by the combination of diurnal nighttime low temperatures and the maximum temperature achieved at each potential failure site (solder joint, component lead, and so on) as a result of diurnal daytime high temperatures, cooling system performance, operational cycles, and equipment power on-off cycles.

Experience on programs where durability fatigue analyses have been conducted and validated shows that the temperature cycling fatigue contribution is typically 80 to 90 percent of the total. This is true even for platforms with relatively severe vibration environments.

Vibration and temperature cycling environments are orthogonal to each other

Circuit Card Assembly (CCA) *vibration* fatigue (primarily component leads and solder joints) is typically due to the flexure perpendicular to the plane of the CCA: As the CCA flexes repeatedly, the strains imposed on the component leads and solder joints lead to the accumulation of fatigue damage.

CCA temperature *cycling* fatigue (again, primarily component leads and solder joints) is due to Coefficient of Thermal Expansion (CTE) mismatch between the component and the CCA in the plane of the CCA: As the CCA goes through repeated thermal cycles, the strains imposed on the component leads and solder joints lead to the accumulation of fatigue damage.

Changes to improve performance in one endurance/durability/life environment can degrade performance in the other. For example, stiffening the card to improve vibration performance could degrade performance in temperature cycling. It follows that long life in one durability environment does not imply any life in the other.

Environmental stress screening

As previously noted, the intent of ESS is to precipitate infant mortality (latent manufacturing) flaws so that they can be repaired, and the fielded item will be at the beginning of the flat portion of the bathtub curve.

A longstanding industry "rule of thumb" holds that Power Spectral Density (PSD) levels below 0.04 g^2/Hz are insufficient to precipitate flaws.

Another industry rule of thumb holds that ESS should not consume more than 5 percent of the demonstrated endurance/durability/life of the item. This is to increase the probability that the item remains on the flat portion of the bathtub curve for its planned useful life.

Table 1 makes use of the equation from MIL-HDBK-810F, Paragraph 2.2 Fatigue Relationship, to determine the percentage of demonstrated durability life consumed by ESS on a hypothetical program. For this hypothetical program, ESS is performed for 10 minutes at 0.04 g^2/Hz. Durability vibration testing is conducted for five hours (300 minutes) at different levels depending on the item installation zone. In this hypothetical case, conducting ESS for items installed in installation zones with PSDs of 0.04 g^2/Hz or higher might make sense, assuming that the items have infant mortality defects. For items installed in the zones with lower PSDs, the conduct of ESS is non-value added, meaning that the field/durability vibration level is too low to precipitate any infant mortality defects. It is also deleterious to the items' reliability, as an excessive portion of demonstrated durability vibration life is consumed.

If the unit had to repeat (there is no limit to how many times this could happen) the last five minutes of vibration after failure correction, then well over 100 percent of demonstrated useful life would have been consumed.

Again, for the hypothetical program, an endurance/durability/life temperature cycling requirement is not specified. Even assuming that there are no repeated cycles following correction of a failure, at least 100 percent of demonstrated useful life has been consumed when ESS is completed. In the absence of an endurance/durability/life temperature cycling requirement, one pass through ESS is all that is included in the demonstrated temperature cycling durability life. If there are repeated ESS cycles, then the situation would be considerably worse.

In this case, the bathtub curve is shown in Figure 2. The actual item might be better than the requirements, but there would be no evidence or data to show that this is the case. The flat portion of the bathtub curve, where our reliability predictions have some validity, does not exist. The inherent reliability of the unit has been degraded by the fatigue damage it has accumulated. In the case of vibration, this was done in the attempt to eliminate latent defects that the field level is too low to precipitate.

ESS is an attempt to "inspect in" quality for low production rate equipment. Defects in high production rate equipment can be reduced or eliminated by the application of statistical process control and automation. High production rate equipment is far more likely to be COTS than custom military specification design. It follows that COTS is far more likely to be defect free than custom military specification design.

How program/equipment managers can avoid these pitfalls

One way to decompose reliability is into two questions. First, is the item inherently robust enough? (Endurance/durability/life environments address this.) Second, is the item defect free? Boeing has experience flying COTS items such as Ricoh printers, Sony satellite dish receivers, and HP servers on military-derivative aircraft without conducting ESS. In this relatively benign environment of commercial aircraft converted to a military application, COTS items have proven considerably more reliable than the military specification Government Furnished Equipment (GFE). These COTS items are clearly not robust enough for severe environment platforms such as fighter aircraft, but their reliable performance on military-derivative aircraft confirms that ESS would be non-value added since field experience has shown these items to be relatively free of infant mortality defects. In addition, given that the items were not designed for flight environments, ESS would be more likely to degrade reliability by consuming an excessive portion of their durability life.

- Durability environments must include vibration and temperature cycling requirements consistent with the planned usage and planned useful life.
- ESS vibration and temperature cycling must be limited, in each case, to some small portion (typically 5 percent) of demonstrated life, including a specified number of allowed repeat/repair cycles.

Vibration						
ESS			Durability			Percent of demonstrated life consumed by ESS
Duration (Minutes)	PSD (g^2/Hz)	Duration x PSD^4	Duration (Minutes)	PSD (g^2/Hz)	Duration x PSD^4	
10	0.04	2.56E-05	300	0.002	4.8E-09	99.98%
				0.004	7.68E-08	99.70%
				0.008	1.2288E-06	95%
				0.016	1.96608E-05	57%
				0.032	0.000314573	8%
				0.040	0.000768	3%
				0.064	0.005033165	1%
				0.128	0.080530637	0.03%

Table 1 | The equation from MIL-HDBK-810F, Paragraph 2.2 Fatigue Relationship, is used to determine the percentage of demonstrated durability life consumed by ESS on a hypothetical program.

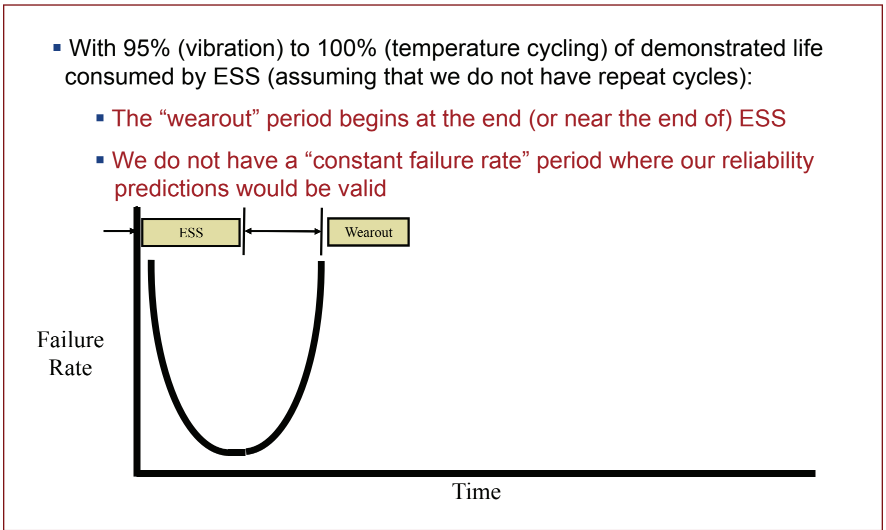

Figure 2 | This bathtub curve shows 95 to 100 percent of demonstrated life consumed by ESS.

- Vibration ESS should not be conducted when the durability vibration level is too low to precipitate infant mortality defects.
- ESS should not be conducted on items (typically COTS) shown to be free of infant mortality defects.

The proper application of qualification, ESS, and reliability prediction methods, avoiding the system engineering pitfalls described herein, will minimize total ownership cost while enhancing effectiveness for the warfighter.

James A. Robles *is a Boeing Senior Technical Fellow working in electronic packaging disciplines including system architectures, avionics hardware design, mechanical tolerance analysis, thermal and dynamic/vibration analysis, weights/mass properties analysis, design of experiments, environmental analysis and test, reliability, and environmental stress screening. He leads the ITAA working group for EIA-933 Standard for Preparing a COTS Assembly Management Plan. Additionally, James is the Boeing Focal for VITA, developing open standards for next-generation COTS assemblies for military/aerospace applications. He can be reached at James.A.Robles@boeing.com.*

The Boeing Company
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www.boeing.com

A longer version of this article is available at www.mil-embedded.com/articles/id/?3839.

Obsolete semiconductors: A proactive approach to End-of-Life

By George Karalias

One thing that's inevitable in military electronics is semiconductor obsolescence. But is there a way to plan for EOL – thereby obsoleting obsolescence and avoiding gray market practices while limiting risk before it's too late.

As electronic technology advancements continue to accelerate, semiconductor life cycles continue to shorten. The average life cycle of a typical semiconductor device is approximately three years, which includes introduction, design-in, production, low-volume, and End-Of-Life (EOL) phases. Once a manufacturer discontinues a product and an EOL announcement is made, customers typically have 6 to 12 months to decide whether to place a last-time buy, or find an alternative solution.

A semiconductor EOL announcement can create a costly inconvenience for customers, as it can be difficult to accurately forecast last-time buy requirements, absorb the additional inventory and storage costs associated with last-time buys, or find an available drop-in replacement. Because the EOL schedule does not typically support the continuing needs of all of its customers, especially those serving applications with long system life cycles, many companies are left in a difficult position. Their supply chains are interrupted, and they no longer have a reliable component source to meet ongoing production, maintenance, and repair requirements.

Companies supporting applications with long-term service requirements such as government, military, and aerospace, along with other Original Equipment Manufacturers (OEMs), can also find themselves servicing and maintaining a product in the field for years without the support of an original semiconductor manufacturer. Faced with an uncertain supply and a steady demand, a customer might have few choices in finding an alternative source for the discontinued semiconductor, making EOL planning all the more vital.

EOL planning: Obsoleting obsolescence

The discontinuing of semiconductor devices is inevitable. Every product and technology has a life cycle, thus it is only a matter of time before a semiconductor device is discontinued by the manufacturer to make way for the next-generation part. OEMs need to plan ahead for EOL announcements, perhaps implementing the plan as early as the time at which a semiconductor is designed into the end-equipment, to find a suitable new source for the critical semiconductor part (Sidebar 1).

Is it too late?

It is almost never too late to begin working with a contractually licensed semiconductor manufacturer. Although planning ahead is the optimal solution, sometimes EOL announcements are vague or go unheeded, and a customer is in need of a part that no longer exists and for which IP is no longer available. Through unique programs, such as Rochester Electronics' Semiconductor Replication Process (SRP), a device can be reverse-engineered to create an exact replica, delivering a semiconductor with the same specifications and performance as the original. And in some cases, additional capabilities and technologies can even be added to the device to improve performance, rad-hard, and other requirements. All re-creations are authorized by the original manufacturer to eliminate any potential for legal ramifications. Through device re-creation programs, as long as the customer possesses a functioning part, it's never too late to extend the life of a device.

Sidebar 1 | Through unique programs, a device can be reverse-engineered to create an exact replica.

It is not enough for a customer to react to an EOL notification, since by that time a new source of semiconductor devices already needs to be identified and qualified as an authorized source for authentic and reliable parts. It is important for customers to have a proactive mindset for the EOL announcement of critical semiconductor components to ensure continuous manufacturing with traceable, high-quality semiconductors. By implementing an EOL plan, OEMs will have sufficient time to investigate the following options.

Drop-in replacement
A drop-in replacement is a "pin-for-pin" replacement of the original semiconductor device. If supplied by a trusted source, this solution enables a customer to bypass virtually all of the obstacles that the following two options carry.

Authorized continuing source manufacturer
Another solution for many customers is a contractually licensed continuing source manufacturer and authorized distributor of semiconductors to provide a continuous supply of qualified parts. These authorized manufacturers engage with the original semiconductor manufacturer to acquire the remaining inventory, including packaged devices, finished devices, die, selected intellectual property, tooling, test programs, and test equipment, thus extending the life of the semiconductor series. For example, Figure 1 shows an Intel 186 high-performance, low-power processor ideal for embedded applications, available through the Rochester Electronics Extension-of-Life process.

Figure 1 | An Intel 186 high-performance, low-power processor ideal for embedded applications is available through the Rochester Electronics Extension-of-Life process.

"OEMs need to plan ahead for EOL announcements, perhaps implementing the plan as early as the time at which a semiconductor is designed into the end-equipment, to find a suitable new source for the critical semiconductor part."

Such a transfer of technology assures there is no interruption of authorized, certified, and traceable devices in the supply chain. Through contract, these authorized sources will place devices into bonded inventory, where the devices are safely and properly stored in dedicated temperature- and humidity-controlled warehouses, as seen in Figure 2. Products are distributed to specific customers through a customized, comprehensive, scheduled, and managed program. The special product agreement alleviates many of the problems that arise from unplanned EOL events during the course of a critical system's existence, including last-time buy and inventory storage costs.

Figure 2 | Authorized sources will place devices into bonded inventory for a customer, where the devices are safely and properly stored in dedicated temperature- and humidity-controlled warehouses.

Redesigning the system

If a drop-in replacement cannot be procured from the original manufacturer or secondary sources, one option is to redesign the system to eliminate the part, or use a different device in its place. A redesign can be costly due to engineering man-hours and the expense of purchasing new devices as well as from production downtime as the new system goes through retesting and requalification processes. There is also the real possibility that the new device will eventually be unavailable due to an EOL announcement. For many customers, a redesign might not be a feasible option due to costs and the lead time associated with mission-critical board-level certifications such as MIL-PRF-38535, MIL-STD-883, and many more. OEMs who do not plan ahead might be forced to consider unauthorized sources, such as brokers and independent distributors for available excess inventory.

Gray market practices: A risky proposition

The danger of buying components through brokers or independent distributors on the gray market is that there is no guarantee of authenticity, quality, traceability, reliability, and continuous availability of the parts. OEMS have no easy way to ensure that the devices purchased are genuine or that the components have been properly stored and handled to ensure quality and reliability. Counterfeiting – the fraudulent manufacturing, distributing, and selling of fake or replica semiconductors – is a growing problem throughout the electronics industry. As counterfeiters become more sophisticated, the probability of receiving re-marked devices increases. These devices could include falsified part numbers or company logos, empty devices with no die, falsified paperwork/RoHS compliance, and counterfeit chips.

Counterfeiting devices has a negative effect on reputable component manufacturers and distributors, causing purchasing dilemmas for component buyers, problems for equipment manufacturers, and trouble for equipment operators. In a worst-case scenario, counterfeit components can cause legitimate manufacturers to be driven out of business or experience catastrophic disasters through equipment failure. For mission-critical applications such as military and aerospace, there can be even more serious consequences: Faulty equipment can result in loss of life. An OEM who believes a part is faulty or counterfeit should immediately report problems to the original semiconductor supplier.

Limiting risk

To limit risk when purchasing obsolete semiconductors, consider cost instead of pricing. Even if a bargain is available for semiconductor devices from an unauthorized source, one must consider the overall cost of manufacturing downtime and/or failure of the end-product if the part turns out to be faulty or counterfeit. These costs far outweigh the front-end savings, not to mention the incalculable cost of damage to the company's reputation.

There are only two fail-safe ways to ensure that a semiconductor device purchased is legitimate: 1) buying directly from the original manufacturer; or 2) enlisting the help of authorized distributors and manufacturers. No amount of testing and screening can give 100 percent assurance when devices are purchased from unauthorized sources. The practices of planning ahead and developing a partnership with an authorized source ensure a continuous stream of genuine devices for the foreseeable future.

The bottom line

Planning ahead for a semiconductor EOL announcement as early as during the OEM product design process can simplify a potentially troubling semiconductor procurement situation and save the OEM money. By partnering with authorized distributors or the manufacturer, the life of the once-discontinued part can be extended, and the OEM can avoid forecasting last-time buys and incurring inventory storage costs. These partnerships also allow the OEM to bypass dealing on the risky gray market, where procuring faulty and counterfeit parts could cost millions of dollars as a result of manufacturing downtime and the failure of the end-product in the field. Planning ahead for EOL ensures there is no interruption in the OEM's supply chain and that manufacturing can continue with traceable, high-quality semiconductors from a reliable and trusted source.

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Rochester Electronics
978-462-9332
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Editor's Choice Products

Editor's note: Military Embedded Systems *is "hip" to the whole Web 2.0 social networking revolution. While we don't know which of today's buzzy trends will last, we're going to start including links to vendors' social networks, when provided. You can also reach us on Twitter, Facebook, and LinkedIn ... and that's just for this week. Next week there'll undoubtedly be more new sites.*

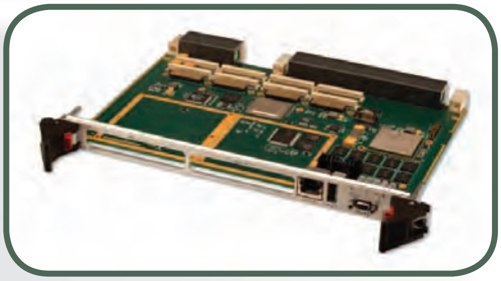
Supercomputing applications get all things in one (mostly, anyway)

What if one technology could offer it all – and be everything for everyone? While that's attempting the impossible, GE Intelligent Platforms has come pretty darned close. Its GRA111 graphics platform is available in 3U VPX style, yet is also OpenVPX compatible. What more could be needed? Glad you asked. The platform also features NVIDIA Corporation's CUDA general-purpose parallel computing architecture, along with NVIDIA's GT 240 GPU. GE says GRA111 is "the first rugged implementation of a CUDA-capable GPU" and is designed to render supercomputing capabilities to video surveillance, signals intelligence, and radar applications. How: GE reports that an unnamed military prime contractor achieved a 15x improvement with CUDA "with minimal reprogramming effort" for a radar application.

In addition to its CUDA architecture featuring the CUDA Instruction Set Architecture (ISA), the GRA111 achieves its need for speedy computing with the help of a 1,302 MHz GT 240 GPU processor clock, a 540 MHz graphics clock, 1 GB DDR3 video memory, 96 cores, a 16-lane PCI Express Gen 2 interface, and a 128-bit memory interface. GRA111 also includes sensor data input capabilities utilizing video formats such as NTSC, RS170, or PAL.

GE Intelligent Platforms • www.ge-ip.com • RSC# 43835

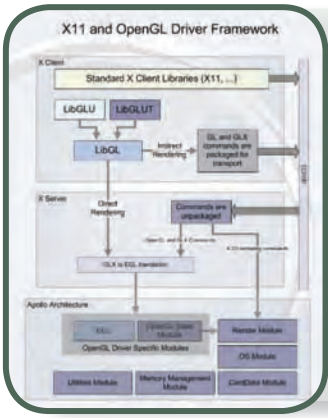
SBC offers 'Extreme' versatility



Versatility is indeed a coveted quality within the spectrum of modern embedded technologies. And … Extreme Engineering Solutions, with its XCalibur 1541, has versatility down to a science: The 6U VPX SBC proffers capabilities suitable for a wide range of applications, including everything from commercial and military to industrial. Geared toward low-power, high-performance systems, XCalibur1541 features a Freescale MPC 8572E PowerQUICC III processor with two e500 Power Architecture cores tucked inside, running at up to 1.5 GHz. Not only that, two PrPMC/XMC interfaces also boost this SBC's versatility factor.

Meanwhile, other notables of the XCalibur1541 include up to 256 MB NOR flash and up to 4 GB NAND flash, in addition to 4 GB DDR2-800 ECC SDRAM in two channels. I/O includes two USB ports, two SATA 3.0 ports, and four GbE ports. Since it all has to run on enabling software, here we go again with the versatility factor: OS support includes: Linux BSP, QNX Neutrino BSP, Wind River VxWorks BSP, and Green Hills INTEGRITY BSP. And if you run into any issues or have any questions, Extreme Engineering guarantees all technical inquiries will be answered within a four-hour window. Now that sounds almost as magical as the SBC's Arthurian legend namesake.

Extreme Engineering Solutions, Inc. • RSC# 43178 • www.xes-inc.com



X11 server meets – and integrates use of – RTOSs

Seems that today, most military embedded front-line and intelligence-gathering technologies run on some sort of RTOS. And it hasn't always been easy to use or host RTOS-based systems on the server, integral as they are, because of their innate complexity. However, ALT Software's Embedded X11 Server aims to solve these issues via its unique environment that supports X11 applications empowered by OpenGL. The purpose: to render easy-to-use GUIs in addition to X API-based legacy 2D application interfaces, all with the intent to provide X-Windows and RTOS interoperability. Myriad CPU and GPU possibilities are supported, as are Green Hills' INTEGRITY and Wind River's VxWorks RTOSs. The company also reports that porting the server to additional platforms is no problem.

The Embedded X11 Server is deployed in stand-alone configurations, or it can be integrated with OpenGL graphics drivers from ALT Software. The stand-alone configuration route affords customers improved functionality and performance through direct graphics processor rendering access, along with hardware initialization. The Embedded X11 Server also features acceleration of both 2D and 3D graphics and the capability for simultaneous execution of several applications.

ALT Software Inc. • www.altsoftware.com • RSC# 44155

Ultra-compact AC/DC power module powers 'em up

Face it. No matter which fabulous boards, software, or even components are in an application or system, they all mean absolutely nothing without … power. And in today's SWaP-constrained mil embedded world, what could be better than an ultra-compact AC/DC power module like RECOM Power, Inc.'s new RAC20-SB to bring the application or system to life. Measuring a mere 52.4 mm (2.06") in length, 27.2 mm (1.07") in width, and 23.5 mm (.93") in height, this small package packs a powerful punch of up to 20 W within the mid-power range. It can also be slipped in where the 5 W model left off as the two modules are pin compatible.

The RAC20-SB is made to work on universal mains that have 90 to 264 VAC input voltages and are also vended with 3.3 V, 5.0 V, 12 V, 15 V, and 24 V output voltages. The miniscule no-load consumption of these modules hovers under 500 mW, in compliance with the EU's existing 2010 "green" power policies and its slated 2013 policies. Though output voltage limits can make efficiency rates vary, the RAC20-SB can rise to 86 percent at 24 V. The device additionally sports a "Class B" filter and features a 3,000 VDC minimum isolation. Ambient temp operating range in free air convection is -40 °C to +70 °C, and RAC20-SB reaches 250,000 hours MTBF in accordance with MIL-HDBK-217F specifications.

RECOM Power, Inc. • www.recom-power.com • RSC# 44154

XMC carrier card cuts complications

In today's stressful, complicated world, it's nice to think that *something* could be easy and without hassle. Thanks to Curtiss-Wright Controls Embedded Computing's VPX3-216 ExpressReach XMC carrier card, the concept of "easy" (or at least *"easier"*) is now a distinct possibility. The switchless carrier is designed to ease XMC mezzanine card integration in three headache-reducing ways. First, it's OpenVPX (VITA 65) compatible. (Need we say more?) Next, it affords one XMC expansion site that is mapped straight to the PCIe backplane fabric, eliminating the need for PCIe switches that add latency and mandate reconfiguration. And finally, of course, it increases its host SBC's I/O capabilities, thereby nullifying the need for more SBCs.

Because the card's only active components are its power controller and IPMI controller, it offers a low-power footprint. Additionally, the VPX3-216 ExpressReach, designed for high-performance military applications, is available in three ruggedization levels: VPX-REDI (VITA 48.1), conduction-cooled (Level 100/200), and air-cooled (Level 0/100). Other highlights include PN5-PN6 connectors, XMC I/O routed according to VITA 46.9 with 38 single-ended signals and 20 differential impedance-controlled pairs, support for x8 lanes PCIe to XMC, and operation at +5 V or +12 V.

Curtiss-Wright Controls Embedded Computing • RSC# 44153 • www.cwcembedded.com

Gloves on a touch-screen computer are … no problem

Soldiers or technicians out in the field are sometimes forced to work in ultra-harsh environments that, in turn, require heavy-duty protective gloves while entering or receiving data from military embedded computing technologies. This is a dicey proposition when using a computer with keys, and even worse on a touch-activated display screen where the opportunity for inexactness (when gloved) is increased. Enter Getac Inc.'s V100 Tablet PC, which the company claims is the first ruggedized touch-screen computer that can be used with or sans gloves.

While many touch-screens have capacitance sensitivity as their basis, this tablet PC doesn't (though the company hasn't revealed what the V100 Tablet PC's sensitivity activation technology *is* based on). But we do know that Getac's tablet PC operates via the user's dual- or single-touch, application, and "flick" gestures, whereby activities such as zoom, copy, move, delete, and rotate are accomplished.

In addition to its command accuracy when gloves are worn, extreme weather condition deployment also require fast reports and high resolution. Accordingly, the V100 Tablet PC provides resolution of 2,048 x 2,048, less than 35 ms response time, and a report rate of 100 points per second. It is also compatible with Microsoft's Windows 7 operating system.

Getac, Inc. • www.getac.com • RSC# 44156

Synchro/Resolver interface board offers choices in 2x2x2

Maybe the engineers at United Electronic Industries (UEI) had the theme of "duos" or "doubles" on their mind when they designed their DNx-AI-255 synchro/resolver interface board. The first set of doubles is manifested in the board's two-channel format, in addition to the board's two models – one for rackmounting within a UEI HalfRACK or PowerDNR RACKtangle chassis and the other for compatibility with UEI's PowerDNA Cubes. Another evidence of the dual mentality: Each board can operate as a simulation output device or as a synchro/resolver input interface. (That's a lot of twos.)

Now to delve deeper: Each board's two synchro/resolver channels are fully isolated and have independent A/D converters. Not only that, each channel provides accuracy of ±2.6 arc minutes, up to 4,000 Hz scan rates, and 16-bit resolution. When the channels are configured as a synchro/resolver simulated output, they are highly suitable for usage in apps such as flight simulation or avionics test systems, as the boards can serve as software-controlled input stimuli. When used in simulator mode, the DNx-AI-255 utilizes an SDR value for the simulated device's position input. Software support is provided for OSs such as VxWorks, Linux, and Windows; application packages including LabVIEW, DasyLAB, and MATLAB; and programming languages like C and C#.

United Electronic Industries • www.ueidaq.com • RSC# 44157

Ada compiler moves up to x86

Though the Ada programming language is primarily used on legacy apps these days, companies devoted to Ada continue to roll out new products to fill a still-existing niche. Case in point: The company formerly known as Aonix recently introduced its ObjectAda Real-Time 8.4 for Windows compiler, designed for use with Intel x86 Pentium architectures and Wind River's VxWorks RTOS. (Aonix merged with Artisan Software Tools in late January, becoming a new entity known as Atego.) Following on the heels of what-was-then Aonix's 2009 introduction of its ObjectAda Real-Time for VxWorks with PowerPC architectures, the x86-oriented 8.4 version comprises an ACATS 2.5 Ada 95 compiler along with supporting tools. ObjectAda Real-Time 8.4 for Windows is also simpatico with the VxWorks environment's cross-development toolset and OS.

Here's how it works: The x86 compiler leverages the Eclipse-based Wind River Workbench development environment, and users can optionally use ObjectAda's command-line or standard graphical interface. ObjectAda VxWorks additionally proffers runtime library support so that developers can execute Ada using Wind River BSPs on Intel Pentium targets. The runtime library also supports the target simulation facility VxSim, which can be executed minus the target hardware – and enables users to execute testing and initial application startup by way of a Windows/Intel host development platform.

Atego • www.Atego.com • RSC# 44158

A 1GHz Fanless Rugged SBC of *EPIC* Proportions

The EPX-855 is a rugged single board computer that provides an open powerful platform for demanding applications. It has a wealth of onboard I/O plus expansion options. Also it supports Linux, Windows® XP embedded, and other x86 real-time operating systems.

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Intel tries DSP again … using a 'soft' approach

By Chris A. Ciufo, Editor

***Editor's note:** The following ran in DSP-FPGA.com just prior to Intel's January onslaught of Core Technology processors at CES. With "over 25 processors and chipsets" on tap, COTS vendors have flooded the market with Core i7 and i5 boards that now do general purpose* and *signal processing in hardware.*

Launched in 1989, the Intel 80860 ("i860XP") digital signal processor set a number of trends for the time but never really achieved commercial market success. Notably, the VLIW architecture included a 32-bit ALU and a three-part 64-bit floating-point processor unit. (At the time, 16-bit CISC CPUs were still shipping in volume.) According to the folks at Answers.com and this writer's first-hand knowledge, the i860 competed for market share and Intel resources against the company's 80960Kx RISC CPUs. Recall that these were the heady days when every major semiconductor company built their own CISC processor and the migration to RISC was an approaching sea change. Intel end-of-lifed the i860 in the 1990s, followed thereafter by the '960 family as well – freeing up the company to focus on the then-recently introduced (and hugely successful) Pentium family. So you could say that Intel's foray into DSP didn't last too long.

Today, of course, DSP is used in practically every digital doodad from MP3 players to smart phones to automotive engine management units. Intel's plans for DSP no longer include discrete, stand-alone devices; rather, DSP is built into the company's Nehalem (Core i7 and follow-on) architecture as well as Intel's System-on-Chip (SoC) product line that started with the EP80579 multimedia processor for set-top boxes and high-end HDTVs. Intel implements DSP in on-chip functional units such as MPEG-4 decoders, WiMAX radios, and various other codecs that deal with audio, imaging, or software-defined radios. But beyond highly integrated Application-Specific Standard Products (ASSPs) based on SoCs, what is the company doing for general-purpose DSP implementations?

Intel is following the same strategy I've postulated with regard to the company's Wind River acquisition: using software to drive chip sales. Its two biggest tactical initiatives are among the best-kept secrets you've probably never heard of: 1) a three-piece PowerPC with AltiVec to Intel Architecture (IA) SSE conversion toolkit, and 2) the FPGA-based QuickAssist Technology.

Partnered with and partially funding the UK company NA Software Limited (NASL), Intel now offers three tools that move AltiVec DSP applications to Intel processors. In the general-purpose DSP market, which includes automotive and what Intel calls Military, Aerospace, and Government (MAG), Freescale's PPC has been the market leader in DSP for more than 10 years. With native signal processing instructions for FFTs and other vector operations built into the AltiVec engine, the PowerPC offered the best balance between general processing ("housekeeping") and signal processing ("number crunching") in a single device.

But Freescale was slow to move to multicore CPUs, and the company's last discrete PowerPC – the MPC8641D dual-core – never gained market traction. This is partly due to Intel's onslaught of dual-core Core Duo and Core 2 Duo CPUs during the past two years. Intel sees it this way: "Problem: AltiVec roadmap products are uncertain. Opportunity: Intel multicore processors are very effective for DSP applications."

I'll say. Using "Tool 1," a VSIPL library for IA, a 1K point FFT is faster on a 2.16 GHz Core Duo 2 than on a 1 GHz 8641D (400 MHz bus) as follows: Real-to-complex: 7.5 versus 4.5 for IA (in microseconds); Complex-to-real: 7.7 versus 4.6 for IA; Complex to Complex out-of-place: 10.9 versus 6.8 (running Linux). For vector routines where the AltiVec really shines, IA was equivalent or better as follows: Vector square root: 1.4 versus 1.3 on IA; Complex vector multiply: 2.4 versus 1.8; and Polar convert: 15.6 versus 10.7. Vector cosine, however, ran slower on IA due to the hardwired instructions in the AltiVec: 3 versus 6.4 on IA. (Note: Code was not optimized for multithreading or multicore on IA. One might expect better results with tweaking.)

"Tool 2" is an altivec.h header file for IA that allows users to take AltiVec code unchanged and convert it to SSE SIMD for SSE2-SSE4 IA processors. By the time you read this, the version for VxWorks 6.6 should be available – do you see how Wind River again plays into Intel's plans? And finally, for PPC designs with lots of hand-coded "bare metal" optimizations (such as loop unrolling), "Tool 3" is an AltiVec Assembler/Compiler for IA. Stuff AltiVec code in one end, turn the crank, and out pops Intel SSE assembler code. Again, Linux and VxWorks versions should be available as you read this.

It's amazing that Intel has never made much noise about these three tools because the implications are huge! You can find more information from NASL or in an Intel webinar at http://edc.intel.com/Video-Player.aspx?id=2315.

As for QuickAssist Technology, Intel has created an API for SSE that bolts off-chip FPGA-based coprocessors to the CPU's FSB. Now turned into a "community" of more than 20 third-party vendors such as XtremeData, Celoxica, and GE Intelligent Platforms, QuickAssist also includes hooks into Intel's next-gen CPU roadmap. I doubt that Intel's getting into the FPGA business anytime soon, but through QuickAssist it has endorsed what the market has already decided: FPGAs are the best way to do flexible and programmable DSP routines.

Add up the impressive DSP on-chip capabilities of IA processors, plus tools that convert from PowerPC legacy designs into IA devices, then toss in direct-connect FPGA coprocessors, and it's clear that Intel is back in the DSP business. In all cases, software remains the key to the company's DSP renaissance.

GE
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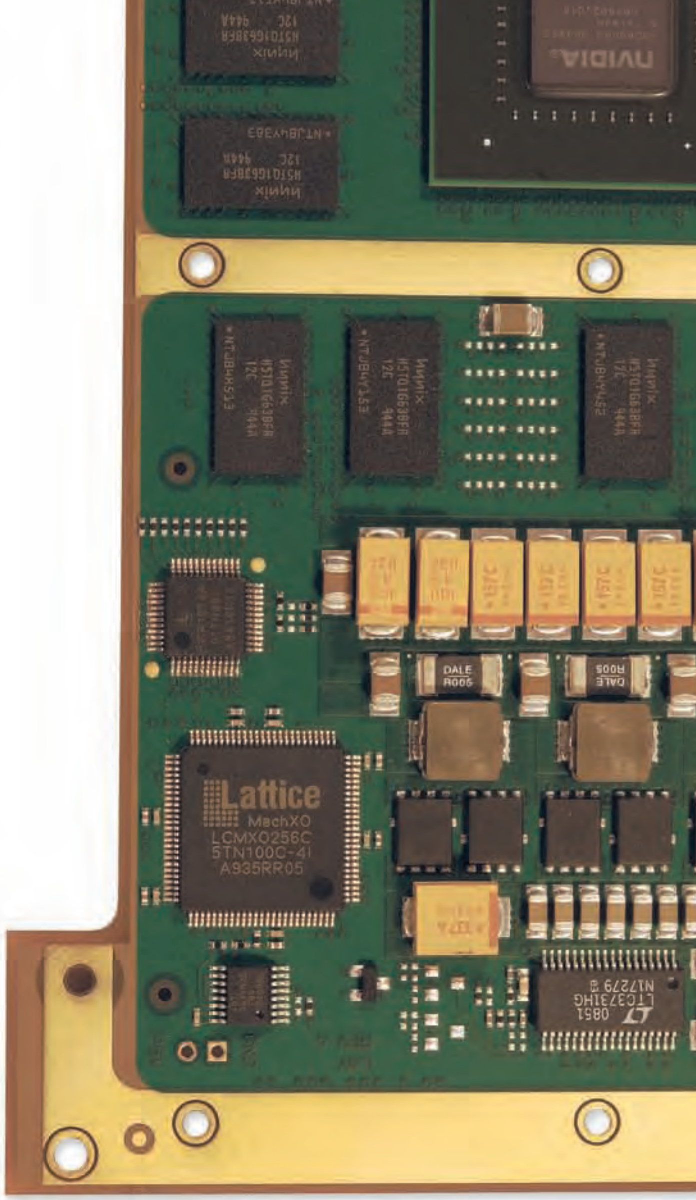

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